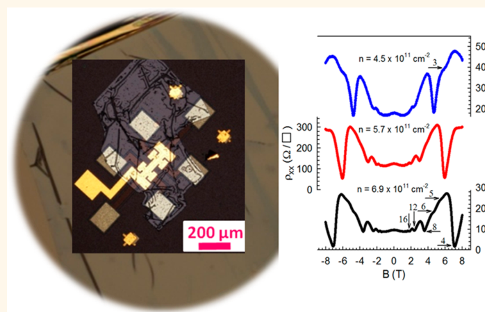
Electronic Transport Properties of Epitaxial Si/SiGe Heterostructures Grown on Single-Crystal SiGe Nanomembranes

Yize Stephanie Li,* Pornsatit Sookchoo, Xiaorui Cui, Robert Mohr,[†] Donald E. Savage, Ryan H. Foote, RB Jacobson, José R. Sánchez-Pérez, Deborah M. Paskiewicz,[‡] Xian Wu, Dan R. Ward,[§] Susan N. Coppersmith, Mark A. Eriksson, and Max G. Lagally*

University of Wisconsin—Madison, Madison, Wisconsin 53706, United States. [†]Present address: Western Digital, Irvine, CA 92612. [‡]Present address: Materials Science Division, Argonne National Laboratory, Argonne, IL 60439. [§]Present address: Sandia National Laboratories, Albuquerque, NM 87185.

ABSTRACT To assess possible improvements in the electronic performance of two-dimensional electron gases (2DEGs) in silicon, SiGe/Si/SiGe heterostructures are grown on fully elastically relaxed single-crystal SiGe nanomembranes produced through a strain engineering approach. This procedure eliminates the formation of dislocations in the heterostructure. Top-gated Hall bar devices are fabricated to enable magnetoresistivity and Hall effect measurements. Both Shubnikov-de Haas oscillations and the quantum Hall effect are observed at low temperatures, demonstrating the formation of high-quality 2DEGs. Values of charge carrier mobility as a function of carrier density extracted from these measurements are at least as high or higher than those obtained from companion measurements made on heterostructures grown on conventional strain graded substrates. In all samples, impurity scattering appears to limit the mobility.



KEYWORDS: SiGe nanomembrane · Si quantum well · two-dimensional electron gas · mobility · Shubnikov-de Haas oscillations · quantum Hall effect

Originally developed for classical electronics,[1,2] strained-Si quantum wells are playing an increasingly important role in quantum electronics.[3] These quantum wells are created when a thin Si layer is heteroepitaxially grown on SiGe: the larger lattice constant of SiGe produces biaxial tensile strain in the Si layer, and the well is formed in the heterostructure conduction band at the Si layer. Quantum bits (qubits) have been demonstrated in such SiGe/Si/SiGe heterostructures.[4−6] Unlike competing materials for quantum electronics, group IV elements have nuclear-spin-zero isotopes, offering the possibility of nearly eliminating the nuclear-spin bath.[7,8] Combining that with the freeze-out of phonons at low temperatures, these Group-IV elements could act in a manner similar to a solid-state vacuum. The term "silicon vacuum" has, in fact, been applied to the system.[9,10]

The assumption for the use of such a label is, of course, structural and morphological perfection, something that remains an elusive goal. The quantum wells used in past studies[3,4,6] were all grown on plastically strain-relaxed SiGe substrates, produced by grading the composition of, and hence the strain in, Si_xGe_{1-x} layers grown heteroepitaxially on bulk Si(001). Such substrates were widely investigated and optimized in the 1990s,[2] with significant more recent advancements in understanding factors that influence the mobility in these 2DEGs.[11−13]

Nevertheless, plastic strain relaxation inherently involves the introduction of misfit dislocations. The resulting threading dislocations will propagate through all the layers and may cause new misfit dislocations at the Si/SiGe interface if the thermodynamic critical thickness of the Si layer is even just slightly exceeded.[14] It is also known that pileups of dislocations associated with the

* Address correspondence to yli499@wisc.edu, lagally@engr.wisc.edu.

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strain grading generate a lateral strain inhomogeneity of micrometer length scale at the SiGe substrate surface that also propagates through subsequently grown heterostructure layers. Such laterally nonuniformly varying strain in the thin Si layer produces lateral variations in the depth in energy of the quantum well, and thus in the energies of electrons bound in the well.

As a second effect, plastic strain relaxation in SiGe also creates small, local (on a micrometer length scale) differences in the crystal orientation normal to the surface, a phenomenon known as mosaic tilt.[2,15,16] Mosaic tilt leads to different step densities on adjacent crystallites on a nominally flat surface. This atomic-scale disorder influences electronic states in the strained-Si quantum well. Unstrained silicon has multiple conduction band minima (valleys) at the same energy.[17] In strained-silicon quantum wells, there are two such degenerate valleys. In principle, sharp quantum well interfaces (to the SiGe layers) lift the valley degeneracy, providing a unique ground state, split from the higher level by 1 meV.[18] Atomic steps at a quantum well interface make the interface less sharp and thereby reduce this separation of states compared with a step-free interface, a deleterious effect for quantum electronics.[18] In quantum wells with random atomic steps of sufficiently small separation, the valley splitting can be quite small and may vary with the lateral position on a wafer.[18,19]

We present here an approach to fabricate SiGe/Si/SiGe heterostructures without these dislocation-induced materials defects. Our approach is based on Group IV nanomembrane (NM) strain engineering technology, in which a fully elastically relaxed single-crystal SiGe sheet is created[20] and transferred to a new host, where it serves as the substrate for the growth of the heterostructure that produces the strained-Si quantum well, in a procedure that is identical to the conventional approach, except that the substrate does not suffer from the potentially deleterious effects of dislocation formation described above.[20] Thus, the key advance is the increased microstructural and morphological control over the SiGe material, and the heterostructures grown on it.

We fabricate gate-defined Hall bars on these heterostructures and characterize the resulting devices both structurally and electronically. X-ray diffraction (XRD) and Raman spectroscopy demonstrate excellent structural quality, without the signature of dislocation-associated features found in the conventional process. Electronic-transport measurements show the formation of a two-dimensional electron gas (2DEG) in the strained-Si layer with a quality sufficient to observe the quantum Hall effect. The charge carrier mobility extracted from measurements on these as yet not optimized heterostructures is at least as good as that measured for strained-Si 2DEGs grown on optimized conventional strain-graded SiGe substrates under identical conditions. The values are above the threshold mobility level ($\sim$40 000 $cm^2/(V\ s)$ at a charge carrier density of $4 \times 10^{11}\ cm^{-2}$) used as a general quality metric for qubit device fabrication. These structural and electronic device properties indicate that a nanomembrane-based approach is viable and perhaps offers a path to improved 2DEG performance.

RESULTS

The essential feature of the NM strain engineering platform is the use of a sacrificial layer that is removed to release the crystalline NM from the rigid host. The approach is possible in any materials system for which a release layer can be found.[21−23] Nanomembrane-based strain sharing techniques in the SiGe system have been developed that enable partial[24] and complete[20] relaxation of single-crystal SiGe sheets without the insertion of misfit dislocations. In the work of Roberts *et al.*,[24] membrane release is used to increase the strain of a very thin, strained-Si layer sandwiched between thicker $Si_{0.68}Ge_{0.32}$ layers grown on conventional (that is, plastically relaxed) $Si_{0.79}Ge_{0.21}$-on-insulator (SGOI). Upon release of the entire structure from its handling substrate (*via* etching of the oxide of SGOI), additional elastic strain sharing occurs, resulting in an increase in the tensile strain from 0.76% to 0.99%, and a remarkable improvement in the 2DEG magnetotransport.[24] This experiment illustrated the effectiveness of elastic-strain sharing in NM-based systems in controlling and influencing electronic band structure.[21] Because the substrate was plastically relaxed SiGe, the transport results included the potential effects of dislocation-induced relaxation mentioned above.

The current study significantly expands on ref 24 in that the material is free of dislocations or their structural consequences.[20] Additionally, the NM process allows the Si layer to be biaxially tensilely strained to an arbitrary tensile strain, by adjusting the composition of the SiGe NM. The lattice constants for Si and Ge are a_{Si} = 5.431 Å, a_{Ge} = 5.658 Å, respectively. For $Si_{1-x}Ge_x$ alloy, the lattice constant as a function of Ge composition, x, is $a_{SiGe} = 5.431 + 0.2x + 0.027x^2$,[25] which at low x deviates only very slightly from Vegard's law.[26,27] The strain in the Si layer is thus readily deducible from the alloy composition. Whereas for quantum electronics, the preferred composition is near 30% Ge, resulting in $\sim$1.2% biaxial strain in the Si layer, in other applications a higher or lower Ge composition may be desirable.[28]

In the work here, we create strained-Si quantum wells with 1.03% and with 1.11% biaxial tensile strains using $Si_{1-x}Ge_x$ (x = 0.27, or 0.29) NM substrates. These values of strain are near the optimum for the Si qubits.

Briefly, the procedure starts with (001) oriented silicon-on-insulator (SOI) as the initial substrate, in which SiO_2 acts as the release layer, and the Si template layer is dislocation-free.[20] We first grow Si/SiGe/Si trilayers on this SOI(001) substrate, keeping all the

layers below their critical thicknesses for dislocation formation, using molecular beam epitaxy (MBE) or chemical vapor deposition (CVD). We then release the trilayers from the host substrate by HF-etching the buried oxide layer, and we remove the outer Si layers to leave a fully elastically relaxed SiGe sheet. This nanomembrane is transferred and bonded to a hydrogen-terminated Si wafer host substrate.

Figure 1 provides a schematic illustration and characteristics of SiGe NMs. Figure 1, panels a and b, respectively, show an optical micrograph and an AFM image of a representative transferred and bonded SiGe NM. The dark lines are wrinkles introduced during transfer. The transport measurements described below are made in the flat regions bounded by the wrinkles. The root-mean-square (rms) roughness of the flat regions in the NMs is typically 0.6−0.7 nm (scan size: 5 μm × 5 μm, 256 samples per line), with correlation lengths ranging from 0.3 to 0.4 μm. After *ex situ* chemical cleaning, the bulk Si substrate hosting the SiGe NM is transferred to an ultrahigh-vacuum-compatible CVD system. The SiGe NM serves as a substrate for the overgrowth of a SiGe buffer layer (≥500 nm), the strained-Si quantum well (10 to 12 nm), a SiGe offset layer (∼33 nm), and finally a thin Si cap layer (∼0.3 nm) to prevent chemical attack of the SiGe layer. A schematic illustration of such a heterostructure is shown in Figure 1c. As heterostructures grown on SiGe NM substrates are free of threading dislocations, misfit dislocations are not expected to form at the interface unless the strained-Si layer reaches the kinetic critical thickness, which is >35 nm for SiGe with ∼30% Ge.[20] The thicknesses of the strained-Si quantum well in our samples are well below this value. Details of the fabrication procedure and structural characterization demonstrating NM crystalline quality and strain state are found in the Methods section.

We also see no inelastic strain relaxation in the Si layer for heterostructures grown on strain graded substrates, even though the thermodynamic critical thickness is much closer to the ∼10 nm Si layer thickness that we grow. With XRD we are able to observe a strain change of as little as 0.05%, and to that extent we can exclude misfit dislocations at the strained-Si/SiGe interface[14] as a contributor to scattering mechanisms in both systems.

Figure 1d shows a typical AFM image of a Si/SiGe heterostructure grown on SiGe NM substrates. Representative surface rms roughness values of a complete NM-based heterostructure range from ∼0.9 to ∼2.3 nm. While the upper value is similar to that obtained on heterostructures grown on strain graded substrates,[11] the lower number is much better. The lateral height−height correlation lengths extracted from the AFM images are of the order of several tenths of micrometers, values comparable to the mean free path (MFP) of electrons at a carrier density of ∼3 × 10^{11} cm^{-2}, as obtained from electron mobility values (see below).

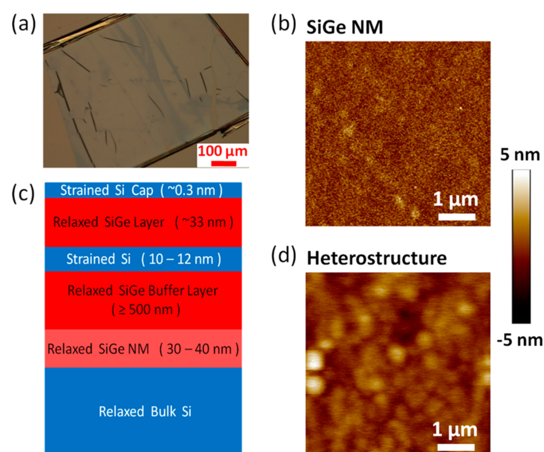

Figure 1. SiGe nanomembrane heterostructures: schematic illustration and characteristics. (a) Optical micrograph of a 32 nm-thick $Si_{0.69}Ge_{0.31}$ NM transferred and bonded onto a bulk Si(001) substrate. The black lines are wrinkles introduced during NM transfer. (b) AFM image of a portion of the transferred SiGe NM shown in (a). The rms roughness is typically 0.6−0.7 nm. (c) Schematic illustration of a Si/SiGe heterostructure grown on a SiGe(001) NM substrate bonded to a hydrogen-terminated Si(001) wafer. Note that the bulk Si, SiGe NM, and the SiGe layers grown by CVD are all at their natural lattice constants. A 1 to 2 nm amorphous interface[29] separating the NM and the bulk-Si(001) host wafer is not shown. (d) AFM image of a portion of a Si/SiGe heterostructure grown on a $Si_{0.73}Ge_{0.27}$ NM substrate. The surface rms roughness is ∼0.9 nm. Height−height correlation lengths range from 0.3 to 0.4 μm.

For charge transport measurements, we fabricate top-gated Hall bar devices on Si/SiGe heterostructures grown on both types of substrates. The effective size of the Hall bar is either 100 μm × 20 μm or 37.5 μm × 3.75 μm. For NM based 2DEGs, the active areas are located on flat regions of the NMs; the bond pads themselves often lie off the NM. Device fabrication and transport measurements are detailed in the Methods section.

Figure 2 summarizes results for a NM based strained-Si 2DEG. Figure 2a shows an optical micrograph of a typical Hall bar device on a NM-based SiGe/Si/SiGe heterostructure. Figure 2b and its inset show the longitudinal resistivity ρ_{xx} as a function of the top-gate voltage V_g at 3 K, illustrating carrier accumulation in the Si quantum well as V_g is increased. A sharp decrease of ρ_{xx} is observed around a threshold gate voltage V_{th}, which is defined empirically as the voltage where the longitudinal resistivity reaches ∼10 kΩ/□, a value within the typical range of critical resistivities for the transition from a nonconducting to a conducting state in 2D systems.[30−33] V_{th} for all the devices we have fabricated, both NM-based and conventional strain-graded ones, lies between 0.5 and 1.5 V. The inset in Figure 2b shows that ρ_{xx} continues to decrease beyond V_{th} as V_g increases.

We perform Hall effect and magnetoresistivity measurements at 3 K and for various top-gate voltages within the range $V_{th} < V_g \leq 3$ V. Representative Hall resistivity (ρ_{xy}) *vs* magnetic-field (B) traces are shown in Figure 2c, for several values of V_g (from top to bottom,

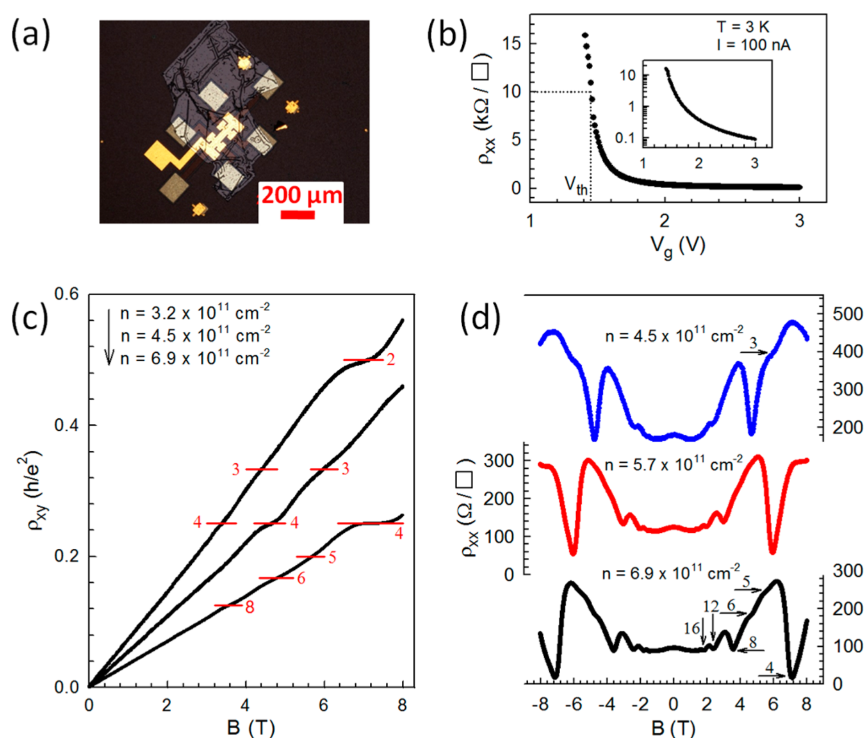

Figure 2. Electronic transport in a NM-based Si/SiGe 2DEG sample (strained-Si layer thickness: ~10.5 nm; Ge concentration: 27%). (a) Optical micrograph of a top-gated Hall bar device. (b) Longitudinal resistivity (ρ_{xx}) as a function of the gate voltage (V_g), illustrating the carrier accumulation process. The threshold voltage, V_{th}, defined empirically as the voltage at which the resistivity is 10 kΩ/□, is indicated by the dotted line. Inset: ρ_{xx} *vs* V_g in a log−linear scale. (c) Transverse resistivity (*i.e.*, Hall resistivity, ρ_{xy}) as a function of the magnetic field at different V_g values, from top to bottom, 2.1, 2.4, and 3.0 V, respectively, showing the linear dependence at low fields and the quantum Hall plateaus at higher fields. The corresponding carrier densities, obtained from a linear fit in the low-field regime, are indicated in the graph. (d) Longitudinal resistivity, ρ_{xx}, as a function of the magnetic field at different carrier densities (the corresponding values of V_g are, from top to bottom, 2.4, 2.7, and 3.0 V, respectively), showing Shubnikov-de Haas quantum oscillations. The Landau level filling factors are indicated for $\nu \leq 16$. The resistivity for the deep minimum at $\nu = 4$ decreases as the carrier density increases and approaches zero at $n = 6.9 \times 10^{11}$ cm^{-2}, because of the increase in mobility arising from better screening at higher electron density. For each carrier density, the *B* values at which the minima or kinks appear in ρ_{xx} *vs B* curves correspond to the *B* values for the Hall plateaus in ρ_{xy} *vs B* curves.

2.1, 2.4, and 3.0 V). The corresponding 2D carrier densities are $n = 3.2 \times 10^{11}$ cm^{-2}, 4.5×10^{11} cm^{-2}, and 6.9×10^{11} cm^{-2}, as determined by the slope of a linear fit to the ρ_{xy} *vs B* curve at low fields. The Hall resistivity shows the emergence of quantum Hall plateaus at higher fields.[34] The Landau-level filling factor for each experimentally detectable plateau, identified by numerically differentiating the trace and locating the field where $d\rho_{xy}/dB \sim 0$, is indicated in Figure 2c. Figure 2d shows the longitudinal resistivity, ρ_{xx}, *vs B*, at $n = 4.5 \times 10^{11}$, 5.7×10^{11}, and 6.9×10^{11} cm^{-2}. The low curvature at zero field and the Shubnikov-de Haas (SdH) quantum oscillations, which progressively become larger at higher fields, indicate that a true two-dimensional electron gas is formed in the strained-Si quantum well.[35] Deep minima, which are evident for all three traces in Figure 2d, indicate Landau levels with filling factors $\nu = 4, 8, ...$ Multiple kinks are also observed in the magnetoresistivity traces, corresponding to Landau levels with $\nu = 3, 5$, and 6, respectively. The sequence of minima/kinks appearing as the magnetic field increases, $\nu = ..., 16, 12, 8, 6, 5, 4, 3, ...$, indicates that the total degeneracy of the states in the well is four (2-fold valley degeneracy and 2-fold spin degeneracy) initially, which is then reduced to two and finally to one as a result of increased spin splitting and valley splitting at increased magnetic field.[36,37] Compared to strain-graded samples, which also exhibit SdH oscillations, the magnetoresistivity traces obtained from NM-based samples consistently have nearly zero curvature at zero field and well-defined oscillation patterns even at low fields (Supporting Information), an indication of excellent two-dimensional electron transport in a single subband.[35]

We now extract the electron mobility, which is an important property of a 2DEG and whose magnitude is a qualitative metric for the performance of Group-IV gate-defined quantum devices.[3] Figure 3 shows a comparison of results along with analysis of the data. Figure 3a shows the mobility as a function of carrier density for two NM-based samples (NM1 and NM2) and three samples grown on conventional strain-graded SiGe substrates from two vendors (Lawrence

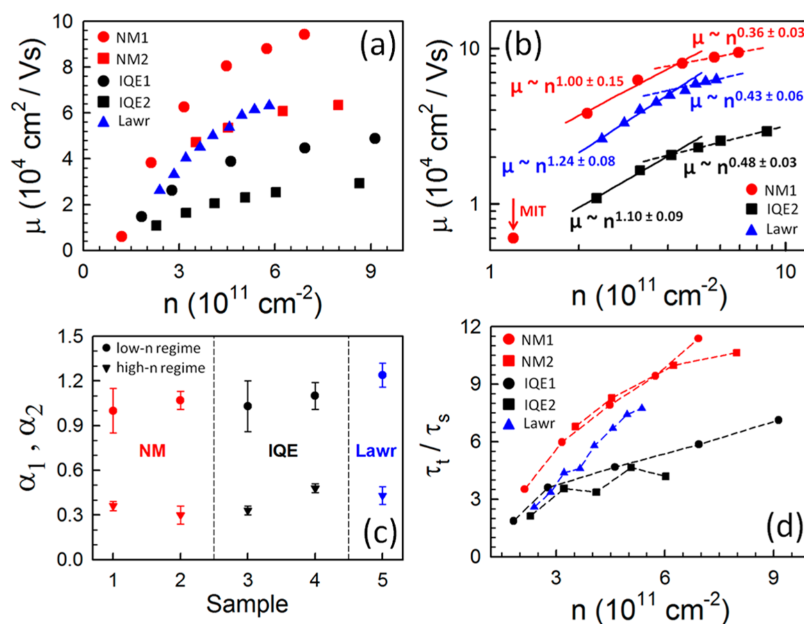

Figure 3. (a) Mobility μ *versus* carrier density n for nanomembrane-based samples (NM1 and NM2) and conventional samples grown on strain-graded substrates from IQE (IQE1 and IQE2) and Lawrence Semiconductor (Lawr). Detailed information about these samples is listed in the Methods section. (b) Mobility *vs* carrier density for NM1, IQE2, and Lawr samples in a log–log scale. Power law function fittings in the low-n regime (solid line) and high-n regime (dashed line) are shown. The data point at the lowest carrier density for NM1, as denoted by "MIT" (for metal–insulator transition), illustrates a deviation from the power law behavior as the critical carrier density for the metal–insulator transition is approached. (c) Powers in the low-n regime and high-n regime for each sample, extracted from the fits to the data in panel (b). (d) Dingle ratio as a function of carrier density for each sample. This number is the ratio between the transport relaxation time and the single-particle elastic relaxation time.[37] The higher Dingle ratio in NM-based samples is evidence of a reduced short-range scattering in these samples.[37]

Semiconductor and IQE) at quite similar conditions. Because of the sensitivity of mobility values to heterostructure parameters and growth/fabrication conditions, such as the strain value, layer thicknesses, and background impurity concentration,[11,12,37,38] it is important that the comparison be made at such similar conditions. The electron mobility obtained for 2DEGs grown on SiGe NM substrates is at least as high, or higher than, that of 2DEGs made on conventional substrates, a promising sign for this NM-based platform. In all cases the mobility shows the same trend with carrier density. The thickness of the strained-Si quantum well layer for all samples is below the thermodynamic critical thickness for misfit dislocation formation. No evidence of relaxation in the Si 2DEG layer is found in the structural characterization, as we have already mentioned. Detailed information about these samples is provided in the Methods section.

For all samples, at low carrier densities, μ increases rapidly with increasing n. This behavior is expected if the dominant effect of increasing n is to enhance the screening of the Coulomb potential from background impurities and/or remote charges at the gate dielectric/semiconductor interface.[11,12,38–40] In Figure 3b we plot the mobility *vs* carrier density in a log–log scale, for three representative samples, NM1, IQE2, and Lawr. In the low-n regime, $n < 5 \times 10^{11}$ cm^{-2}, the μ *vs* n data can be fitted to a power law function $\mu \propto n^{\alpha_1}$, with the power $\alpha_1 = 1.2 \pm 0.1$ for the Lawr sample and $\alpha_1 = 1.0 \pm 0.2$ for all other samples. It has been suggested theoretically[39–41] and verified experimentally[11,42] that, for 2DEG systems, the power is close to 1 if the mobility is limited by background impurity scattering, and is around 1.5 if remote impurity scattering dominates. Although all values are within the range of uncertainty, the slightly higher power in the Lawr sample may suggest a lower background impurity scattering. The electron mean free path (MFP) in this $n < 5 \times 10^{11}$ cm^{-2} regime, as determined by the Fermi velocity and the transport relaxation time, is several hundred nanometers. The deviation from the power law behavior at a very low carrier density (denoted by "MIT" for the data point at the lowest carrier density for NM1 in Figure 3b), is a result, we believe, of a sharp decrease of mobility as the critical carrier density for the metal–insulator transition (MIT) is approached.[12,43–45] In the high-n regime, $n > 5\times 10^{11}$ cm^{-2}, the μ *vs* n data can be fitted to another power law function, $\mu \propto n^{\alpha_2}$, with α_2 in the range 0.3–0.5 for all samples. The powers in low-n and high-n regimes for all five samples are shown in Figure 3c.

The Dingle ratio, which is defined as the ratio between the transport relaxation time (τ_t) and the single-particle elastic relaxation time (τ_s),[37] is computed and plotted as a function of carrier density in Figure 3d for all five samples. This ratio reflects the

relative strengths of long-range and short-range scattering: a large ratio suggests that long-range scattering dominates, otherwise, short-range scattering plays a more significant role.[40] 2DEGs grown on conventional substrates have consistently lower Dingle ratios than those grown on NM substrates, suggesting that short-range scattering is more dominant in conventional samples.

Can we understand these results in terms of a physical picture of operative mechanisms? It is clear that we do not see a dramatic mobility enhancement in NM-based samples. NM based heterostructures are microstructurally much better than strain-graded samples[16] in that they do not contain the effects of misfit dislocations introduced in the growth of the substrate material. As we have pointed out, these effects are threading dislocations, mosaic, and lateral strain variations resulting from dislocation pileup. The density of threading dislocations is so low (10^4 to 10^5 cm^{-2}) that they cannot be important in scattering of charges. Mosaic occurs on the scale of micrometers, and is effectively a different step density in different regions of the growth front. Strain inhomogeneity occurs also on the range of micrometers,[16] with strain variations of 0.1% around the nominal value, which for the substrate is zero.[16]

The most likely cause for the limitations in mobility is the proximity of the top-gate dielectric. This cause is the same for NM based and conventional-substrate based Si 2DEGs. Experimental evidence in our lab, as well as experience by others[46] shows that increasing the offset layer thickness, thus moving the dielectric farther away from the 2DEG, rapidly raises the mobility. The dielectric contains many fixed charges that cause local fields that influence transport. Increasing the offset layer thickness is thus an easy fix for increased mobility; unfortunately doing so is not feasible for quantum electronics, as it makes it much harder to control a qubit. Thus, improving the quality of the dielectric is required if a higher mobility is desired. Efforts are underway locally to do so. Scattering from impurities/fixed charges in the dielectric layer is consistent with the conclusion we reach that impurity scattering limits the mobility.

What is also likely quite similar for both types of substrates is the roughness of the growth front that evolves as the heterostructure is epitaxially deposited. We extract roughness correlation lengths of several hundred nanometers. At the interface between the strained-Si and the SiGe offset layers (top Si/SiGe interface), such roughness translates into a compositionally "rough" region, going from pure Si to the proper SiGe composition over several atomic layers. This laterally and vertically compositionally changing region produces, at least under some circumstances, a lateral strain profile on the scale of the physical growth front roughness. If we assume this interface region has compositionally the same profile as the surface roughness (worst-case scenario), then we can use roughness and correlation length values from the surface to describe the interface strain profile.

Feenstra *et al.* have suggested that in a typical strained-Si 2DEG, the strain modulation associated with interfacial compositional variation on the scale of physical growth front roughness dominates other factors that may limit the mobility.[47] That may be the case here as well. We computed local interface strain variations using a procedure similar to that of ref 47. We obtain variations in the absolute strain (around the nominal value, which here would be the ~1% strain in the Si 2DEG layer) of 0.02% for a sample with rms roughness of 0.9 nm and correlation length of 300 nm. These values are smaller than strain variations due to dislocation pileups in strain-graded substrates, but they occur on a more local scale.

This effect may become limiting if the dielectric-layer problem is eliminated.[47] If so, smoother growth would have to be achieved (something that may be difficult) before the microstructural factors associated with strain-graded substrates become important in limiting the mobility.

CONCLUSIONS

In summary, we report measurements of charge transport in strained-Si 2DEGs fabricated on crystalline-SiGe substrates created using nanomembrane strain engineering methods. In such substrates, only elastic strain relaxation is involved and thus dislocations never play a role. Removing the need for the plastic (*i.e.*, inelastic) strain relaxation that is at the core of the conventionally used substrates removes strain inhomogeneities and mosaic tilt. The nanomembrane approach produces structures that have demonstrably less structural disorder than conventionally strain-graded heterostructures. The resulting 2DEGs have charge carrier mobilities that are at least as high as those of 2DEGs made on conventional samples, but not significantly higher, as we had expected. In both types of samples, the mobility appears to be limited in the same manner. We suggest that the primary cause is the dielectric layer required for making a top gate, which contains many fixed charges. Secondarily, compositional variation at the upper strained-Si/SiGe interface, where the 2DEG resides, created by growth front roughness, will be the same for both types of samples and may limit mobility in the same way in both.

Currently, extended defects and structural imperfections do not appear to play a role in limiting the electron mobility in our samples. We expect a difference in mobilities to appear only if one eliminates fixed charges and defects in the dielectric layer and if one is able to reduce the growth front roughness sufficiently so that the carrier mean free path becomes great

TABLE I. Sample Information for the Hall Bar Devices Studied in this Work

sample	substrate	Ge composition	strain in Si well	Si well thickness
NM1	NM substrate	27% ± 0.5%	1.03% ± 0.02%	10.5 nm
NM2	NM substrate	29% ± 0.5%	1.11% ± 0.02%	10.5 nm
Lawr	Strain-graded substrate (provided by Lawrence Semiconductor Research Laboratory, Inc.)	29% ± 0.5%	1.11% ± 0.02%	10.5 nm
IQE1	Strain-graded substrate (provided by IQE, Inc.)	32% ± 0.5%	1.23% ± 0.02%	11.8 nm
IQE2	Strain-graded substrate (provided by IQE, Inc.)	32% ± 0.5%	1.23% ± 0.02%	10.6 nm

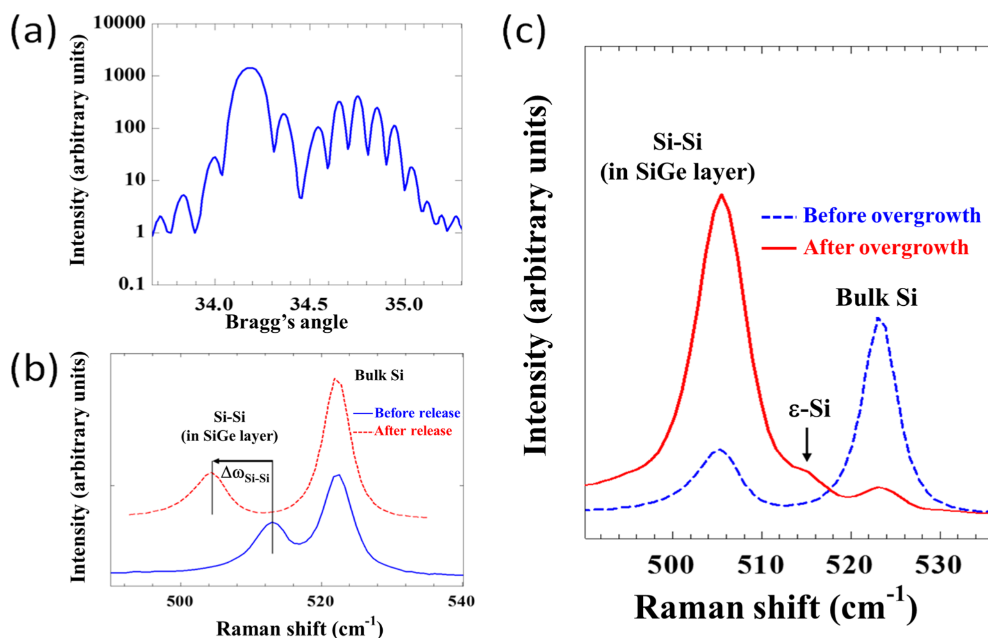

Figure 4. Structural characterization, at various stages of sample fabrication, of Si/SiGe/Si trilayers grown on SOI(001) by MBE. (a) XRD ω-2θ scan along the (004) reflection for an as-grown Si/$Si_{0.77}Ge_{0.23}$/Si trilayer; the thickness of each layer and the Ge concentration are obtained from a fit of the data. (b) Raman spectra for a $Si_{0.69}Ge_{0.31}$ NM before and after release and transfer. The shift of the Si−Si peak, $\Delta\omega_{Si-Si}$, indicates full elastic relaxation of the initial compressive strain in the SiGe layer. (c) Raman spectra for a $Si_{0.69}Ge_{0.31}$ NM before and after growth of a Si/SiGe heterostructure. A strained-Si (ε-Si) peak, with expected frequency shift relative to the bulk-Si peak, appears, as indicated by the arrow.

enough for charges to scatter off more widely separated defects. It is then that NM-based Si 2DEGs will begin to excel.

Typical mobility values in state-of-art strained-Si 2DEGs are sufficiently high for current qubit research. In the future, when multiple qubits are involved, reducing the problems associated with strain graded substrates will become important. It is then that SiGe NM substrates will come into their own as the platform for Si-based quantum electronics.

METHODS

Sample Fabrication. We used the general approach developed in ref 20, with some modifications, to fabricate our samples. The Si/SiGe/Si trilayers were grown on commercial SOI (001) substrates [Soitec, U.S.A.], using molecular beam epitaxy at a temperature of 460 °C, with a growth rate of 0.9 ± 0.1 Å/s for SiGe and 0.6 ± 0.1 Å/s for Si. Typical thicknesses for the SiGe and sandwiching Si layers in the trilayer are 30−40 and 16 nm, respectively. The trilayers were patterned with release holes by standard optical lithography and reactive ion etching. To obtain elastically relaxed SiGe NMs, we first etched away the SiO_2 layer of SOI in 49% HF, and then placed the now freely floating Si/SiGe/Si trilayers into dilute KOH solution, which etched away the outer Si layers. The SiGe NM was rinsed in dionized water, transferred, and bonded to a hydrogen-terminated bulk Si(001) handling substrate. The covalent bonding between the NM and the bulk Si wafer is robust enough to survive chemical cleaning. The interface is a 1 to 2 nm thick amorphous layer.[29] This interface is likely totally irrelevant to the electronic transport in the strained-Si well, as it is more than 600 nm away from the well.

The handling substrate hosting SiGe NMs was chemically cleaned *ex situ* before introduction to the CVD system for the overgrowth of Si/SiGe heterostructures. We first cleaned the substrate with acetone and methanol, and followed by 2 or 3 cycles of (1) ozone oxidization, (2) deionized-water cleaning, and (3) HF dip (to strip oxide on the surface). The CVD growth temperature was 580 °C, and the growth rate was approximately 2 Å/s for SiGe and 0.35 Å/s for Si. The thicknesses of the SiGe buffer layer, the strained-Si well, the SiGe offset layer, and the Si cap layer are 600 nm, 10−12 nm, 33 nm, and 0.3 nm, respectively. Detailed information about the samples, including the Ge composition, strain in the Si well, and the Si well thickness, is listed in Table I.

Structural Characterization. Figure 4a shows a high-resolution X-ray diffraction (HRXRD) $\omega - 2\theta$ scan along the (004) reflection for Si/SiGe/Si trilayers grown by MBE on SOI(001), but not yet released. Sharp thickness fringes, which arise from the interference of X-rays scattered from the surface and interfaces between Si and SiGe layers, indicate that the interfaces are smooth and laterally coherent. In addition, there is no evidence of plastic relaxation *via* misfit dislocations, as there is for strain graded SiGe substrates.[20] The thickness of each layer and the Ge concentration are obtained by fitting the peaks using the RADS MERCURY software.[48] The fitting method is based on dynamical diffraction theory and takes into account the relative peak positions, peak widths, and shapes of the diffraction profile. Figure 4b shows Raman measurements before and after release of a trilayer. The Si−Si peak in SiGe shifts to a lower frequency (relative to its position for the attached trilayer) after release and transfer of the SiGe NM. This frequency shift, which correlates with biaxial in-plane strain through a linear relation,[49,50] is consistent with full elastic relaxation of the initially compressive strain of the SiGe layer in the as-grown Si/SiGe/Si trilayer. After the growth of the Si/SiGe heterostructure, a strained-Si (ε-Si) peak appears in the Raman spectrum (red curve in Figure 4c), as indicated by the arrow. The frequency shift of the ε-Si peak relative to the bulk-Si peak agrees very well with the expected strain state in the Si quantum well as calculated based on the Ge composition determined by XRD.[51]

Device Fabrication and Electronic-Transport Measurement. Top-gated Hall bar devices on Si/SiGe heterostructures grown on SiGe NMs or conventional strain graded substrates are fabricated using standard electron beam lithography. Ohmic contact to the strained-Si layer is achieved through implantation of phosphorus. A 90 nm-thick Al_2O_3 film deposited by atomic-layer deposition (ALD) forms the gate dielectric for the top gate. We fabricate Hall bars of two different sizes: 100 μm $\times$ 20 μm and 37.5 μm $\times$ 3.75 μm. We find that the sheet resistance and the carrier mobility of the 2DEG in the Si quantum well are independent of the Hall bar size in the range of dimensions we used, as expected for a uniform device. Electronic-transport measurements are carried out in a variable-temperature cryostat with a 9 T superconducting magnet (Quantum Design, PPMS). The method we employ here to probe the electronic transport properties is standard for 2DEGs;[34] the results are notable only because we grew the 2DEG heterostructure on a NM.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Section 1, structural issues in conventional samples; Section 2, comparison of SdH oscillations in NM-based and conventional samples. The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/nn506475z.

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